UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,451	09/27/2001	Axel Hertwig	PHDE 000167	5357

24737 7590 04/19/2005

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,451	HERTWIG ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 12 have been examined. Claims 1 – 12 have been rejected.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) in view of Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

3.1. The art of Rothlauf is directed toward an asynchronous multiplexing system ***(Title)***.

3.2. The art of Mano is directed to computer system architecture ***(Title)***, including asynchronous data transfer ***(pages 424 – 426)***.

3.3. Rothlauf appears to teach a multiprocessor array ***(figure 1, items 18, 20, 22, 24, 26, and 28; and column 3, lines 20 -23)***, which includes:

3.3.1. A first processor shadow register unit which operates within a first clock domain ***(figure 1, item 18)***.

3.3.2. At least one second processor shadow register unit ***(figure 1, item 20)***.

3.3.3. A peripheral unit which operates ~~which operates~~ within a peripheral clock domain ***(figure 1, items 10 and 84)***, and includes:

3.3.3.1. A multiplexer unit which is connected to the first shadow register unit and the at least one second shadow register unit so as to transmit data ***(figure 1, item 10)***,

3.3.3.2. A register unit ***(figure 1, item 42)***, the construction of the first shadow register unit and the at least one second shadow register unit and the register unit being identical in respect of function, and

3.3.3.3. A priority unit ***(figure 1, items 96, 98, 100, and 102)***, for allocating the multiplexer unit for data transmission to the first shadow register unit or to the at least one second shadow register unit ***(figure 1, items 96, 98, 100, and 102)***, the priority unit being connected so as to transmit data to the first shadow register unit and to the at least one second shadow register unit ***(figure 1, items 96, 98, 100, and 102)***.

3.4. Rothlauf does not specifically teach:

3.4.1. A first processor shadow register unit which operates within a first clock domain and includes:

3.4.1.1. ***A first processor, and***

3.4.1.2. ***A first shadow register unit which is connected to the first processor so as to transmit data, and***

3.4.2. At least one second processor shadow register unit which:

3.4.2.1. ***Operates within a corresponding second clock domain, and***

3.4.2.2. ***Includes a second processor, and***

3.4.2.3. ***A second shadow register unit which is connected to the second processor so as to transmit data.***

3.5. Mano appears to teach a processor shadow register unit which operates within a clock domain ***(page 424, starting at paragraph 4, through page 426 until section First-In First-Out; and figure 11-12, the CPU plus asynchronous communication interface is described)*** and includes:

3.5.1.1. A processor ***(page 424, starting at paragraph 4, through page 426 until section First-In First-Out, the CPU described)***, and

3.5.1.2. A shadow register unit which is connected to the processor so as to transmit data ***(page 424, starting at paragraph 4, through page 426 until section First-In First-Out; and figure 11-12, the asynchronous communication interface described)***.

3.6. Rothlauf and Mano are analogous art because they are both contain the same problem area of asynchronous data transfer ***(Mano, page 423, header of the page labeled "Asynchronous Data Transfer")***.

3.7. The motivation to combine the art of Mano with the art of Rothlauf would have been obvious given the need expressed in Rothlauf for data terminals with universal asynchronous receiver transmitters (UART's) ***(Rothlauf, figure 1, items 18 – 28; and column 1, lines 22 – 35; and column 3, lines 20 – 37)***, and the data terminal solution provided in Mano ***(Mano, pages 424 – 426, and figure 11-12; please note that an asynchronous communication interface is functionally equivalent to a universal asynchronous receiver transmitter (UART) – please refer to page 424, paragraph four, last sentence)***.

3.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Rothlauf to produce the invention of claim 1.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

4.1. Claim 2 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

4.2. Rothlauf does not specifically teach that a first shadow register unit, the at least one second shadow register unit and the register unit include status flags as well as control/data registers.

4.3. Mano appears to teach that a first shadow register unit, the at least one second shadow register unit and the register unit include status flags as well as control/data registers ***(figure 11-12, items labeled status register, control register, and transmitter register)***.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

5.1. Claim 3 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

5.2. Rothlauf does not specifically teach that the first clock domain and/or the at least one second clock domain include more than one processor.

5.3. Mano appears to teach a clock domain with more than one processor ***(page 458, figure 11-34)***.

5.4. Rothlauf and Mano are analogous art because they are both contain the same problem area of digital logic components used to construct digital equipment such as multiplexers and data terminals.

5.5. The motivation to combine the art of Mano with the art of Rothlauf would have been obvious given the benefit expressed in Mano of improved system performance ***(Mano, page 454, paragraph four that starts with, "The benefit . . .")***.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

6.1. Claim 4 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

6.2. Rothlauf appears to teach that in order to read out data from the first shadow register unit and/or the at least one second shadow register unit the multiplxer unit is connected thereto in the read out direction ***(figure 1, items 54 and 58)***.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

7.1. Claim 5 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

7.2. Rothlauf appears to teach that requests for access from the first shadow register unit and/or the at least one second shadow register unit to the priority unit are encoded as a one-bit signal ***(figure 1, item 62; and column 3, lines 46 - 49)***.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

8.1. Claim 6 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

8.2. Rothlauf appears to teach that the priority unit grants priority to the first shadow register unit or the at least one second shadow register unit in conformity with the principle: first-come, first-served ***(column 1, lines 58 – 64; please note the phrase "data words are transmitted in an asynchronous manner determined by the sequence in which such data words are formed")***.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

9.1. Claim 7 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

9.2. Rothlauf appears to teach that the priority unit grants priority to the first shadow register unit or to the at least one second shadow register unit in conformity with the principle: all shadow register units are served successively ***(column 2, lines 7 – 12)***.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall) in view of Schwartz (Schwartz, Mischa; "Telecommunication Networks: Protocols, Modeling and Analysis", 1987, Addison-Wesley).

10.1. Claim 8 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

10.2. The art of Rothlauf is directed to an asynchronous multiplex system ***(Title of patent)***, including the area of polling ***(column 4, lines 4 – 8)***.

10.3. The art of Schwartz is directed to telecommunications networks ***(Title of book)***.

10.4. Rothlauf does not specifically teach that the priority unit grants priority to the first shadow register unit or to the at least one second shadow register unit in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit.

10.5. Schwartz appears to teach that the priority unit grants priority to the first shadow register unit or to the at least one second shadow register unit in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit ***(page 408, section 8-1-1 Roll-call Polling, first paragraph, especially the sentence that starts with "Stations may be polled more than once during a cycle")***.

10.5.1. Regarding ***(page 408, section 8-1-1 Roll-call Polling, first paragraph, especially the sentence that starts with "Stations***

may be polled more than once during a cycle"); this is functionally equivalent to statistically allocating a given percentage of time for accessing the peripheral unit. Also, please note that the method of scanning the shadow registers described in Rothlauf is functionally equivalent to allocating an equal percentage of time to each shadow register.

10.6. The art of Schwartz and the art of Rothlauf are analogous art because they both contain the problem of polling to control access to a peripheral resource.

10.7. The motivation to use the art of Schwartz with the art of Rothlauf would have been obvious because of the suggestion in Scwartz that polling can be based on priority considerations or respond to variations in traffic ***(page 408, section 8-1-1 Roll-call Polling, first paragraph, especially the sentence that starts with "Stations may be polled more than once during a cycle")***.

10.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Schwartz with the art of Rothlauf to produce the invention of claim 8.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer

System Architecture", 1982, Prentice-Hall) in view of Dodley (U.S. Patent 5,966,229).

11.1. Claim 9 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

11.2. The art of Rothlauf is directed to an asynchronous multiplexer system ***(Title of patent)***, including communication system ***(column 2, lines 55 – 68; column 3, lines 1 – 20; column 4, lines 26 – 30)***.

11.3. The art of Dodley is directed to a free-space optical communication system ***(Title of patent)***.

11.4. Rothlauf does not specifically teach that the peripheral unit is constructed as an infrared device, UART interface or USB interface.

11.5. Dodley appears to teach an infrared interface ***(column 1, lines 29 – 34)***.

11.6. The art of Dodley and the art of Rothlauf are analogous art because they both contain the problem of communication systems.

11.7. The motivation to use the art of Dodley with the art of Rothlauf would have been obvious given the need in Rothlauf for a communication line ***(column 2, lines 55 – 68; column 3, lines 1 – 20; column 4, lines 26 – 30)***.

11.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Rothlauf to produce the invention of claim 9.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall) in view of Artwick (Artwick, Bruce A.; "Microcomputer Interfacing", 1980, Prentice-Hall).

12.1. Claim 10 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

12.2. The art of Rothlauf is directed toward an asynchronous multiplexing system ***(Title)***.

12.3. The art of Artwick is directed to interfacing microcomputers to peripheral devices ***(Title)***, including asynchronous data transfer devices ***(pages 202 – 205)***.

12.4. Rothlauf does not specifically teach that the first shadow register unit and/or the at least one second shadow register unit are connected to the associated processor via an interrupt.

12.5. Artwick appears to teach that the first shadow register unit and/or the at least one second shadow register unit are connected to the

associated processor via an interrupt ***(page 204, paragraph 3, last sentence; page 205, figure 5-11, line number 7 labeled Interrupt Request; please note the use of an asynchronous communications interface in claim 1 to provide the shadow register; also please note that it is obvious that an interrupt line is used to interrupt the processor)***.

12.6. The art of Artwick and the art of Rothlauf are analogous art because they both contain the problem area of digital logic components used to construct digital equipment such as multiplexers and data terminals.

12.7. The motivation to use the art of Artwick with the art of Rothlauf would have been obvious given the need expressed in Rothlauf for data terminals with universal asynchronous receiver transmitters (UART's) ***(Rothlauf, figure 1, items 18 – 28; and column 1, lines 22 – 35; and column 3, lines 20 – 25)***, and the asynchronous communication interface provided in Artwick ***(pages 202 – 205, and figure 5-11; please note that an asynchronous communication interface is functionally equivalent to a universal asynchronous receiver transmitter (UART) as discussed in claim 1)***.

12.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Artwick with the art of Rothlauf to produce the invention of claim 10.

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall).

13.1. Claim 11 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

13.2. Rothlauf appears to teach a communication terminal using the multiprocessor array as claimed in claim 1 ***(figure 2, item 14, note: item 14 is functioning as a communication terminal which utilizes items 10 and 16 which are the multiprocessor array)***.

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rothlauf (U.S. Patent 4,325,147) and Mano (Mano, Morris, M.; "Computer System Architecture", 1982, Prentice-Hall) in view of Pride (Pride,William M.; Hughes, Robert J.; Kapoor, Jack R.; "Business", 1996, Houghton Mifflin Co.).

14.1. Claim 12 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

14.2. The art of Pride is directed to business methods, including computer hardware ***(page 503, section Computer Hardware and Software)***, and future computer applications ***(page 512, section Future Computer Applications)***.

14.3. Rothlauf does not specifically teach a portable device using the multiprocessor array as claimed in claim 1.

14.4. Pride appears to teach a portable device ***(page 514, picture; page 522, picture)***.

14.5. The art of Rothlauf and the art of Pride are analogous art because they both contain the problem of data terminals communicating with a master station ***(Rothlauf, column 1, lines 5 – 10)*** and ***(Pride, page 506, section labeled "Computer Networks")***.

14.6. The motivation to use the art of Pride with the art of Rothlauf would have been obvious because of the benefits recited in Pride for using a portable device, such as determining the value of inventory ***(page 514, picture and caption)***, and getting the job done with portable computers even during lunch ***(page 522, picture and caption)***.

14.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Pride with the art of Rothlauf to produce the claimed invention.

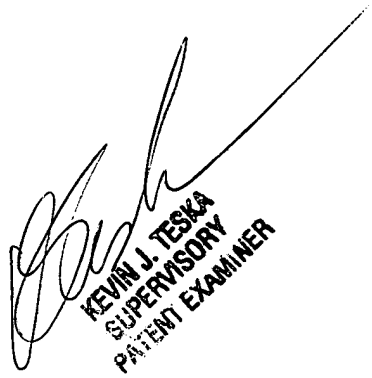
Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone

number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



RG